

AMENDMENT

Serial Number: 10/022,628

Filing Date: December 17, 2001

Title: METHOD AND APPARATUS FOR SCHEDULING PACKETIZED DATA FLOWS IN A CALENDAR-BASED
ARBITRATION SCHEME

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IN THE CLAIMS

Please amend the claims as follows:

1 1. (Currently Amended) An arbitration unit, comprising:
2 an allocation unit ~~that~~to assigne a first number of slots in a frame to a first flow and a
3 second number of slots in the frame to a second flow; and
4 a scheduling unit ~~that~~to assigns first slot positions to the first number of slots in the frame
5 and second slot positions to the second number of slots in the frame using a binary distribution
6 tree, wherein the scheduling unit includes a plurality of modules, each including a divider, a
7 module memory capable of identifying an output previously assigned a first remainder, and an
8 adder capable of adding a second remainder to a number allocated to an output previously not
9 assigned the first remainder.

1 2. (Original) The arbitration unit of Claim 1, wherein the first flow and the second flow
2 are flows of discrete packets.

1 3. (Original) The arbitration unit of Claim 1, wherein the binary distribution tree
2 generates a binary permission vector (BPV) for each of the first and second flows.

1 4. (Currently Amended) ~~The arbitration unit of Claim 1~~An arbitration unit, comprising
2 an allocation unit to assign a first number of slots in a frame to a first flow and a second
3 number of slots in the frame to a second flow; and
4 a scheduling unit to assign first slot positions to the first number of slots in the frame and
5 second slot positions to the second number of slots in the frame using a binary distribution tree,
6 wherein the scheduling unit comprises a plurality of modules, each of the plurality of module
7 divides an allocation number by two between two outputs of the module, and assigns any
8 remainder between one of the two outputs that had not most recently been assigned a previous
9 remainder.

1 5. (Canceled) The arbitration unit of Claim 1, wherein the scheduling unit comprises a
2 plurality of modules, each including:
3 a divider;

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4 a module memory that is capable of identifying an output which was previously assigned
5 a first remainder; and
6 an adder that is capable of adding a second remainder to a number allocated to an output
7 that had previously not been assigned the first remainder.

1 6. (Currently Amended) The arbitration unit of Claim 5~~1~~, wherein the divider divides a
2 binary number by two by stripping off the lower-order bit of the binary number.

1 7. (Currently Amended) The arbitration unit of Claim 5~~1~~, wherein the module memory
2 comprises:
3 a toggle flip-flop;
4 a plurality of gates that perform an ANDing function; and
5 an inverter.

1 8. (Currently Amended) ~~The arbitration unit of Claim 1.~~ An arbitration unit, comprising
2 an allocation unit to assign a first number of slots in a frame to a first flow and a second
3 number of slots in the frame to a second flow; and
4 a scheduling unit to assign first slot positions to the first number of slots in the
5 frame and second slot positions to the second number of slots in the frame using a binary
6 distribution tree, wherein the binary distribution tree comprises ~~comprises~~ includes P levels of modules,
7 where 2^P is the maximum number of slots assignable to any frame.

1 9. (Original) The arbitration unit of Claim 8, wherein each module has two
2 corresponding outputs.

1 10. (Original) The arbitration unit of Claim 9, wherein each module in the binary
2 distribution tree comprises:
3 a divider that divides an input number evenly between outputs of a module; and
4 a module memory that is capable of selecting which of the outputs of the module to transmit a
5 remainder.

1 11. (Original) The arbitration unit of Claim 10, wherein the module memory is
2 configured to alternate transmission of the remainder between the outputs of the module.

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1 12. (Original) The arbitration unit of Claim 8, further comprising a vector processing
2 unit that converts a plurality of binary permission vectors into a single integer permission vectors.

1 13. (Original) The arbitration unit of Claim 12, wherein the vector processing unit
2 comprises a plurality of counter modules.

1 14. (Original) The arbitration unit of Claim 8, wherein a first level of scheduling module
2 is capable of processing an allocation number corresponding to a first flow while a second level
3 of scheduling module is processing an allocation number corresponding to a second flow.

1 15. (Original) A method for generating binary permission vectors, comprising:
2 setting a common drift direction at bifurcation points in a binary distribution tree;
3 dividing allocation numbers associated with a first flow by two at the bifurcation points;
4 assigning quotients from the dividing of the allocation numbers associated with the first
5 flow to branches at the bifurcation points;
6 assigning a remainder from the dividing of the allocation numbers associated with the
7 first flow to a branch that corresponds to a drift direction at the bifurcation point where the
8 remainder exists;
9 switching the drift direction at the bifurcation point where the remainder exists; and
10 reading outputs from the binary distribution tree as elements in a first binary permission
11 vector.

1 16. (Original) The method of Claim 15, wherein setting the common drift direction at
2 the bifurcation points in the binary distribution tree comprises assigning a leftward drift to
3 scheduling modules on a scheduling unit.

1 17. (Original) The method of Claim 15, wherein dividing the allocation numbers
2 associated with the first flow comprises dividing an allocation number of the first flow and
3 dividing values generated from dividing the allocation number of the first flow.

1 18. (Original) The method of Claim 15, further comprising:

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2 dividing allocation numbers associated with a second flow by two at the bifurcation
3 points;
4 assigning quotients from the dividing of the allocation numbers associated with the
5 second flow to the branches at the bifurcation points;
6 assigning a remainder from the dividing of the allocation numbers associated with the
7 second flow to a branch that corresponds to a drift direction at the bifurcation point where the
8 remainder exists;
9 switching the drift direction at the bifurcation point where the remainder exists; and
10 reading the outputs from the binary distribution tree as elements in a second binary
11 permission vector.

1 19. (Original) The method of Claim 18, wherein the dividing of allocation numbers
2 associated with the second flow is performed concurrently with the dividing of allocation
3 numbers associated with the first flow.

1 20. (Original) The method of Claim 18, further comprising generating an integer
2 permission vector from the first binary permission vector and the second binary permission
3 vector.

1 21. (Currently Amended) An arbitration unit, comprising:
2 means for assigning a first number of slots in a frame to a first flow and a second number
3 of slots in the frame to a second flow; and
4 means for assigning first slot positions to the first number of slots in the frame and
5 second slot positions to the second number of slots in the frame using a binary distribution tree,
6 wherein the binary distribution tree includes P levels of modules, where 2^P is the maximum
7 number of slots assignable to any frame.